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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,590	03/01/2004	Todd P. Lukanc	H1775	9600

61060 7590 05/18/2007

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WHITMORE, STACY	
ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
05/18/2007	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/790,590
Filing Date: March 01, 2004
Appellant(s): LUKANC ET AL.

Robert A. Voigt, Jr.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 7, 2007 appealing from the Office action mailed October 23, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,735,742	HATSCH	5-2004
US 2003/0229868	WHITE	12-2003

US 2002/0140920 Rosenbluth 10-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 1-4, 6-9, 12-18, 20 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over White et al. (US Patent Application Publication 2003/0229868) in view of Hatsch (US Patent 6,735,742).

2. As for the claims White discloses the invention substantially as claimed, including:

Claim 1, White et al. disclose a method of designing an integrated circuit (IC) device having desired electrical characteristics, said method comprising:

providing an initial IC device design (Fig.2, element 36, paragraph [0118]);

generating a layout representation corresponding to the initial IC device design (Fig.2, element 36, paragraph [0118] ; Figs. 10A-10C; paragraph[0144]);

simulating how structures within the layout representation will pattern on a wafer (Figs. 10B-10C; paragraph[0144]);

based on the simulating step, determining whether actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics (paragraph[0144]); wherein the desired electrical characteristics include at least one of drive current, gain and switching speed (paragraphs [0006] and [0201]); and

if the actual electrical characteristics associated with the initial IC device design do not sufficiently match the desired electrical characteristics, modifying the initial IC device design (Figs. 10B-10C; paragraphs[0144], [0006], [0014], and [0141]).

White does not specifically disclose that desired electrical characteristics include at least one of only gain and switching activity.
Hatsch discloses desired electrical characteristics of at least one of gain and switching activity [col. 2, line 59 – col. 3, line 16; col. 14, lines 35-40].

It would have been obvious to one of ordinary skill in the art to combine the teachings of White and Hatsch because adding Hatsch's desired characteristics of gain and/or switching speed would have improved White's system by optimizing layouts for functional capability and desired requirements concerning critical paths which would improve design and circuit performance [see Hatsch, col. 3, especially lines 1-16, and 43-51].

Claim 2, White et al. disclose the method of claim 1, wherein the step of determining whether the actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics includes:

determining actual dimensions of structures within the layout representation based on the simulating step (paragraph[0112]-[0114]; [0135]); and

determining the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation (paragraph[0138] and [0144]).

Claim 3, White et al. disclose the method of claim 2, wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using a look-up table (Fig. 25; paragraph [0211]).

Claim 4, White et al. disclose the method of claim 2, wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using an electrical modeling program in which the actual dimensions of the structures are input (paragraphs [0047], [0140], and [0147]).

Claim 6, White et al. disclose the method of claim 1, wherein the step of generating a layout representation corresponding to the initial IC device design includes minimizing the scale of the layout representation (paragraph[0009]).

Claim 7, White et al. disclose the method of claim 1, wherein the initial IC device design includes a desired relationship between at least two structures within the IC device design (paragraph[0115]).

Claim 8, White et al. disclose the method of claim 7, further comprising:

determining an amount of process-related variation associated with at least two structures within the Layout representation of the IC device design (paragraphs[0112]-[0115]).

Claim 9, White et al. disclose the method of claim 8, wherein determining an amount of process-related variation associated with at least two structures within the Layout representation includes:

simulating how structures within the layout representation will pattern on a wafer (paragraphs[0135]-[0138]); and

measuring a feature of the simulated structures, said feature being indicative of process-related variation (paragraphs[0135]-[0138]).

Claim 12, White et al. disclose the method of claim 9, said method further comprising:

measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity (Fig. 3; paragraphs[0120]-[0121] and Fig. 60A; paragraphs[0306]).

Claim 13, White et al. disclose the method of claim 12, wherein the simulated structures are at different locations within the layout representation (Fig. 42; paragraph [0255]).

Claim 14, White et al. disclose the method of claim 9, wherein simulating how structures within the layout representation will pattern on a wafer includes simulating how structures within the layout representation will pattern as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design (Fig. 25; paragraph[0211]; paragraph[0168]), (iii) orientation of a structure, (iv)placement of a structure within a portion of the IC

device design, and (v) size of a structure with respect to other adjacent structures (Fig. 25; paragraph[0211]).

Claim 15, White et al. disclose the method of claim 9, further comprising: determining whether at least a portion (paragraph[0009]) of the IC device design is optimized with respect to process-related variations (paragraph[0304]).

Claim 16, White et al. disclose the method of claim 15, further comprising:

if a portion of the IC device design is not optimized with respect to process-related variations, modifying at least a portion of the IC device design (paragraphs[0009],[0304], and [0135]) .

Claim 17, White et al. disclose the method of claim 16, wherein modifying at least a portion of the IC device design includes modifying at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design (paragraph [0142), (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures (paragraph [0142).

Claim18, White et al. disclose the method of claim 9, wherein the process-related variations include variations caused by at least one of (i) mask generation (paragraph (0112), (ii) wafer patterning, (iii) pre-patterning processing, and (iv) post-patterning processing.

Claim 20, White et al. disclose an integrated circuit (IC) device designed by the method of claim 1 (paragraph [006]).

Claim 31, White et al. disclose a computer-implemented method in which an initial integrated circuit (IC) device design is provided, said method comprising:

generating a layout representation corresponding to the initial IC device design (Fig.2, element 36, paragraph [0118] ; Figs. 10A-10C; paragraph[0144]);

simulating how structures within the Layout representation will pattern on a wafer (Figs. 10B-10C; paragraph[0144]);

based on the simulating step, determining an amount of process-related variation in how at least a portion of the layout representation will pattern on a wafer (paragraph[0009], [0137], and[0144]); and

determining whether the layout representation will pattern as an IC device having desired electrical characteristics (Fig. 10B, paragraph[0144]); wherein the desired electrical characteristics include at least one of drive current, gain and switching speed (paragraphs[0006] and [0201]).

3. Claims 10-11, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over White et al. in view Hatsch (US Patent 6,735,742), and further in view of Rosenbluth et al. (US Patent Application Publication 2002/0140920).

4. As for the claims White in vie of Hatsch discloses the invention substantially as claimed, including:

Claim 10, White in view of Hatsch discloses substantially all the elements in claims 10-11, and 19 as rejected in claims 1, and 7-9 above,

White further discloses Claim 19, the method of claim 11, further comprising:

providing feedback to a designer regarding how a given structure will print on a wafer (White, paragraph [0224]) as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures (White, paragraphs [0115],[0178],[0220] and [0224]).

White in view of Hatsch does not specifically disclose

wherein the feature indicative of process-related variation is at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity.

Claim 11, the method of claim 10, wherein:

a larger slope of edge intensity or logarithm of slope of edge intensity is indicative of a smaller process-related variation; and

a smaller slope of edge intensity or logarithm of slope of edge intensity is indicative of a larger process-related.

Rosenbluth discloses wherein the feature indicative of process-related variation is at least one of (i) slope of edge intensity (paragraphs [0015] and [0019]) and (ii) logarithm of slope of edge intensity (paragraph [0099]);

Claim 11, the method of claim 10, wherein:

a larger slope of edge intensity or logarithm of slope of edge intensity is indicative of a smaller process-related variation (Rosenbluth, paragraphs[0019] and [0082]); and

a smaller slope of edge intensity or logarithm of slope of edge intensity is indicative of a larger process-related variation (Rosenbluth, paragraphs[0019]and [0082]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of White in view of Hatsch with the method disclosed by Rosenbluth because such combined method includes slope of edge intensity / logarithm of slope of edge intensity would provide a technique for optimally choosing illumination distribution and mask features (paragraph [0021]).

(10) Response to Argument

Argument 1 (pages 4-6)

Appellant argues in substance that Examiner's motivation for modifying White (which teaches reducing variations in fabricated chips) with Hatsch to include the missing claim limitation of claims 1 and 31 (desired electrical characteristics include at least one of gain and switching activity) is insufficient to establish a prima facie case of obviousness.

As to Appellant's Argument 1, Examiner respectfully disagrees with for the following reasons.

First, as stated in the final office action dated October 23, 2006, it would have been obvious to one of ordinary skill in the art to combine the teachings of White and Hatsch because adding Hatsch's desired characteristics of gain and/or switching speed would have improved White's system by optimizing layouts for functional capability and desired requirements concerning critical paths which would improve design and circuit performance [see Hatsch, col. 3, especially lines 1-16, and 43-51]. White and Hatch are both directed to the design of integrated circuits, including design prior to fabrication of the integrated circuit (such as in White, abstract, paragraph 0006, fig. 2, element 36 – layout design). White, especially in paragraph 0006, discloses the physical verification of the electronic design (layout), as numerous portions discussing the adjusting of electronic design for improving manufacturability, circuit performance, and even the geometries of electrical features. Hatsch is also concerned with the design and verification of circuit design, and even that of the physical layout and design requirements (col. 2, line 59 – col. 3, line 16; col. 14, lines 20-40). The optimization parameter of switching speed used by Hatsch is a parameter that is related to the layout of the circuit design and component dimensions, ultimately a part of a circuit design wherein signals are transferred along signal paths, which directly affect circuit performance. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of White and Hatch by utilizing Hatch's optimization parameter of switching speed in order to design a circuit with performance being the objective.

Second, prior to the final office action, the independent claims had the limitation of wherein the desired electrical characteristics include at least one of drive current, gain and switching speed wherein White et al. disclose the drive current (paragraphs [0006] and [0201]). Appellant subsequently removed the drive current, and disclosed no criticality concerning the remaining electrical characteristics.

Argument 1 (footnote) (page 6)

Appellant requests that examiner respond to a hypothetical example.

As to Argument 2, Examiner respectfully disagrees with applicant because the argument is directed to subject matter which is not claimed or related to appellant's subject matter, and is therefore irrelevant to the present claimed subject matter.

Argument 2a (page 7)

Appellant argues in substance that White and Hatsch do not disclose wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using a look-up table.

As to argument 2a, examiner respectfully disagrees for the following reasons:

White discloses wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using a look-up table (fig. 25, element 644; paragraph 0211, here White discloses that a look up table is used to map (associate and/or determine) layout features (actual electrical characteristics).

Argument 2b (pages7-8)

Appellant argues in substance that White and Hatsch do not disclose wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using an electrical modeling program in which the actual dimensions of the structures are input.

As to argument 2b, examiner respectfully disagrees for the following reasons: White discloses wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using an electrical modeling program in which the actual dimensions of the structures are input [paragraphs 0047, 0140, and 0147; also fig. 53 and paragraph 0285 where the design specification is provided (input) by a user).

Argument 2c (page 9)

Appellant argues in substance that White and Hatsch do not disclose wherein the step of generating a layout representation corresponding to the initial IC device design includes minimizing the scale of the layout representation.

As to argument 2c, examiner respectfully disagrees for the following reasons:

White discloses wherein the step of generating a layout representation corresponding to the initial IC device design includes minimizing the scale of the layout representation [paragraph 0009, sub-portions; paragraphs 0006-0008, 0118, and 0137 showing that the initial design is a layout representation and that subsequent modifications correspond the initial design. Generating the adjusted designs is

performed on sub-portions of the circuit (layout), which is a minimization of the scale of the original layout.

Argument 2d (pages 9-10)

Appellant argues in substance that White and Hatsch do not disclose wherein the initial IC device design includes a desired relationship between at least two structures within the IC device design.

As to argument 2d, examiner respectfully disagrees for the following reasons:

White discloses wherein the initial IC device design includes a desired relationship between at least two structures within the IC device design [paragraphs 0006, 0115, and 0118, 0140, and 0141 where relationships between features, geometries, structures of the IC design are shown to have desired feature dimensions and relations].

Argument 2e (page 10)

Appellant argues in substance the White and Hatsch do not disclose determining an amount of process-related variation associated with at least two structures within the layout representation of the IC device design.

As to argument 2e, examiner respectfully disagrees for the following reasons:

White discloses determining an amount of process-related variation associated with at least two structures within the layout representation of the IC device design [paragraph 0112-0113 showing that the process related variations, both physical and

electrical for layout patterns (structures) are modeled; paragraphs 0135, 0137-0138, and 0140 showing that process related variations in a process model are used to determine or predict or simulate layout structures within the layout of the IC design].

Argument 2f (page 11)

Appellant argues in substance that White and Hatsch do not disclose measuring the feature indicative of process related variation for one or more simulated structures over a process window of focus and intensity.

As to argument 2f, examiner respectfully disagrees for the following reasons:

White discloses measuring the feature indicative of process related variation for one or more simulated structures over a process window of focus and intensity [paragraph 0138, where White discloses that the features indicative of process variations are simulated, and then physically measured].

Argument 2g (pages 11-12)

Appellant argues in substance that White and Hatsch do not disclose wherein simulating how structures within the layout representation will pattern on a wafer includes simulating how structures within the layout representation will pattern as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures.

As to argument 2f, examiner respectfully disagrees for the following reasons:

White discloses wherein simulating how structures within the layout representation will pattern on a wafer includes simulating how structures within the layout representation will pattern as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures [paragraph 0138 shows that the layout representation is simulated to predict manufacturing variations that will occur, these manufacturing variations are further detailed to include at least one of, if not all of appellant claimed limitations of (i) – (v) in paragraphs 0112-0115, especially paragraph 0115, where the feature dimensions of features that are patterned on a wafer include size, spacing between structures, critical dimensions, and paragraph 0133 where feature density is shown to occur as a result of the manufacturing process. All of these types of situations are included in the simulation model to try and predict and improve the way an IC is manufactured.].

Argument 2h (pages 12-13)

White and Hatsch do not disclose wherein modifying at least a portion of the IC device design includes modifying at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures.

As to argument 2h, examiner respectfully disagrees for the following reasons:

White discloses wherein modifying at least a portion of the IC device design includes modifying at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures [paragraph 0138 shows that the layout representation is simulated to predict manufacturing variations that will occur, these manufacturing variations are further detailed to include at least one of, if not all of appellant claimed limitations of (i) – (v) in paragraphs 0112-0115, especially paragraph 0115, where the feature dimensions of features that are patterned on a wafer include size, spacing between structures, critical dimensions, and paragraph 0133 where feature density is shown to occur as a result of the manufacturing process. All of these types of situations are included in the simulation model to try and predict and improve the way an IC is manufactured. Further is paragraphs 0139-0144 show that the results of the simulation process are used to make improvements, and corrections (modify) to the model or design or layout design, which are iteratively improved to meet design and electrical rules and specifications].

Argument 2i (page 14)

Appellant argues in substance that White and Hatsch do not disclose wherein the process related variations include variations caused by at least one of (i) mask

generation, (ii) wafer patterning, (iii) pre-patterning processing, and post-patterning processing.

As to argument 21, examiner respectfully disagrees for the following reasons:

White discloses wherein the process related variations include variations caused by at least one of (i) mask generation, (ii) wafer patterning, (iii) pre-patterning processing, and post-patterning processing [paragraph 0138 shows that the layout representation is simulated to predict manufacturing variations that will occur, these manufacturing variations are further detailed to include at least one of, if not all of appellant's claimed limitations of (i) – (v) in paragraphs 0112-0115, especially paragraph 0115, where the feature dimensions of features that are patterned on a wafer include size, spacing between structures, critical dimensions, and paragraph 0133 where feature density is shown to occur as a result of the manufacturing process. Paragraph 0140 shows both pre and post patterning processing; Further paragraphs 0147-0149 show the difference between mode A and mode B, where mode A is geared towards mask generation, and mode B is geared towards feature dimension variations, or wafer patterning effects].

Argument B1 (pages 14-18)

First, appellant argues that examiner's motivation for modifying White with Rosenbluth (because such combined method includes slope of edge intensity / logarithm of slope of edge intensity would provide a technique for optimally choosing illumination distribution and mask features (paragraph [0021]).to include the missing

claim limitations of claims 10-11 is insufficient to establish a prima facie case of obviousness.

Second, appellant argues that there is no language in Rosenbluth (and in particular [paragraph 0021]) that makes any suggestion that wherein the feature indicative of process-related variation is at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity; or that a larger slope of edge intensity or logarithm of slope of edge intensity is indicative of a smaller process-related variation; and a smaller slope of edge intensity or logarithm of slope of edge intensity is indicative of a larger process-related variation.

As to the First argument, examiner respectfully disagrees for the following reasons:

White in view of Hatsch discloses the method of designing the IC having desired electrical characteristics, determining an amount of process related variation associated with at least two structures within the layout, simulating how the structures will pattern, and measuring a feature of the simulated structures, see especially cited in examiner's response to arguments 2e-2g above. Examiner cited Rosenbluth for the claim limitations of wherein the feature indicative of process-related variation is at least one of (i) slope of edge intensity (Rosenbluth, paragraphs [0015] and [0019]) and (ii) logarithm of slope of edge intensity (Rosenbluth, paragraph [0099]); wherein a larger slope of edge intensity or logarithm of slope of edge intensity is indicative of a smaller process-related variation (Rosenbluth, paragraphs [0019] and [0082]); and a smaller slope of edge intensity or logarithm of slope of edge intensity is indicative of a larger process-

related variation (Rosenbluth, paragraphs[0019]and [0082]). In the cited portions Rosenbluth was used to show slope edge intensity, a logarithm of slope edge intensity, and that in paragraph 0099, the log-slope of edge intensity is inversely indicative of slope edge intensity values (or a smaller logarithmic slope edge intensity value shows a larger process related variations, and vice versa). The slope edge intensities are part of a lithography process used in manufacturing integrated circuits. Although White in view of Hatsch does not specifically disclose appellant's claimed limitations related to the slope edges, the cited portions of Rosenbluth utilize process related parameters of slope edges to determine how features will be imaged during the patterning process for the integrated circuit. It therefore would have been obvious to one of ordinary skill in the art at the time the invention was made to combine White in view of Hatsch and Rosenbluth because utilizing slope edge intensities and logarithm of slope edges to show that values are indicative of process related variations in White in view of Hatsch would also be useful in the determination of process variations for White in view of Hatsch's purpose of improving the design (modeling) and manufacture of integrated circuits.

As to the second argument, examiner respectfully disagrees for the following reasons:

Rosenbluth discloses wherein a feature indicative of process-related variation is at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity; or that a larger slope of edge intensity or logarithm of slope of edge intensity is indicative of a smaller process-related variation; and a smaller slope of edge intensity or

logarithm of slope of edge intensity is indicative of a larger process-related variation [paragraphs 0002, 0015, 0019, 0082, and 0099]. Slope edge intensities, and logarithms of the slope edge intensities are process related variations that result from the imaging of features of an integrated circuit during the design and/or the manufacture of integrated circuits or masks which aid in the improvement of lithography tools/processes to ensure that integrated circuits are manufactured properly.

Argument 2a (pages 18-19)

Appellant argues in substance that White, Hatsch, and Rosenbluth do not disclose wherein the (simulated) feature indicative of process related variations is at least one of (i) slope edge intensity and (ii) logarithm of slope edge intensity.

As to argument 2a, examiner respectfully disagrees with appellant for the following reasons:

White discloses the simulation of process related variations with respect to the design of integrated circuits and masks (see as cited in examiner's response to arguments 2f-2h above. Rosenbluth was cited for the addition of the at least one of (i) slop edge intensity and (ii) logarithm of slope edge intensity [see as cited in the examiner's response to (Argument B1, first and second arguments above, including reasons for combination).

Argument 2b (page 19)

Appellant argues in substance that White, Hatsch, and Rosenbluth do not disclose a larger slope edge intensity or logarithm of slope edge intensity is indicative of a smaller process-related variation; and a smaller slope edge intensity or logarithm of slope edge intensity is indicative of a larger process-related variation.

As to argument 2b (page 19), examiner respectfully disagrees for the following reasons:

Rosenbluth discloses a larger slope edge intensity or logarithm of slope edge intensity is indicative of a smaller process-related variation; and a smaller slope edge intensity or logarithm of slope edge intensity is indicative of a larger process-related variation [see as cited in the examiner's response to argument (B1 (pages 14-18), first and second arguments) above].

Argument 2c (page 20)

Appellant argues in substance that White, Hatsch, and Rosenbluth do not disclose providing feedback to a designer regarding how a given structure will print on a wafer as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures.

As to argument 2c (page 20), examiner respectfully disagrees with appellant for the following reasons:

White discloses providing feedback to a designer regarding how a given structure will print on a wafer as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures [see examiner's response to arguments 2g-2h above; and also exemplary fig. 52A, especially GUI based results; fig. 52b, GUI based results; fig. 55, element 2660; fig. 56, element 2699; fig. 57, output from element 2810 going to the users inputs 2800, 2822; White's figures show that the process of determining how features will print on a wafer including the claimed limitations of (i) – (v) are feedback to the designer from improvements to be made during the design process.

(11) Related Proceeding(s) Appendix

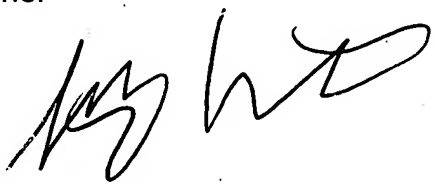
No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Stacy Whitmore

Primary Examiner



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